II. AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) A Rake receiver comprising a radio signal receiving stage, an analogue-to-digital converter (ADC) coupled to the receiving stage, the ADC output being coupled to an input of each of a plurality of parallel signal paths each of the parallel signal paths including signal processing means, combining means for combining outputs from the signal paths and means for recovering symbols from the combined outputs, the receiver further comprising code generation means for generating a filtered pilot code that provides a multibit interpolation of a generated pilot code prior to the parallel signal paths, the filtered pilot code further having out-of-band harmonics removed, and the signal processing means in each of the parallel signal paths comprising a variable delay means for delaying a signal in that path by a desired amount and a means for correlating the delayed signal with the filtered pilot code.

2. (Previously Presented) A Rake receiver as claimed in claim 1, wherein the signal processing means includes signal deriving means coupled to an output of the code generation means and to the variable delay means for deriving an early-late timing error signal for the signal path, wherein the timing error signal is supplied to means for both adjusting the variable time delay of the variable delay means and for deriving an amplitude and phase of the received signal in the respective signal path, and the timing

error signal is further supplied to means for multiplying the delayed signal from the variable delay means by the complex conjugate of the amplitude and phase of the received signal and applying the result to the combining means.

3. (Previously Presented) A Rake receiver as claimed in claim 2, characterised in that the code generation means comprises early, on-time and late outputs of the filtered pilot code, and the signal deriving means comprises, first, second and third correlators, each of the first, second and third correlators having first and second inputs, the first inputs being coupled to an output of the variable delay means and the second inputs being connected respectively to the early, on-time and late outputs of the code generation means, a differencing circuit having inputs connected respectively to outputs of the first and third correlators and an output for the early-late timing error signal, and the second correlator having an output for the amplitude and phase of the received signal in the signal path.

4. (Previously Presented) A Rake receiver as claimed in claim 2, characterised in that the code generation means comprises early, on-time and late outputs of the filtered pilot code and the signal deriving means comprises differencing means having inputs connected respectively to the early and late outputs of the code generation means, first and second correlators, each of the first and second correlators having first and second inputs, the first inputs being coupled to the output of the variable delay means and the second inputs being connected respectively to the on-time output of the code generation

means and to an output of the differencing means, the first correlator having an output for the amplitude and phase of the received signal in the signal path and the second correlator having an output for the early-late timing error signal.

5. (Previously Presented) A Rake receiver as claimed in claim 2, characterised in that the code generation means comprises early and late outputs of the filtered pilot code and the signal deriving means comprises first and second correlators, each of the first and second correlators having first and second inputs, the first inputs being coupled to the output of the variable delay means and the second inputs being connected respectively to the early and late outputs of the code generation means, differencing means having inputs coupled respectively to outputs of the first and second correlators and an output for the early-late timing error signal and combining means having inputs coupled respectively to outputs of the first and second correlators and an output for the amplitude and phase of the received signal in the signal path.

6. (Previously Presented) A Rake receiver as claimed in claim 2, characterised in that the code generation means comprises fixed delay means and the signal deriving means comprises first, second and third correlators, each of the first, second and third correlators having first and second inputs, the first input of the first correlator being coupled to the output of the variable delay means, first and second differential delay means having inputs coupled to the output of the variable delay means and outputs coupled respectively

to the first inputs of the second and third correlators, the first differential delay means delaying the output of the variable delay means by half a chip period and the second differential delay means delaying the output of the variable delay means by a chip period, second inputs of the first, second and third correlators being coupled to an output of the code generation means, a differencing means having inputs connected respectively to outputs of the first and third correlators and an output for the early-late timing error signal, and the second correlator having an output for amplitude and phase of the received signal in the signal path.

7. (Previously Presented) A Rake receiver as claimed in claim 3, characterised in that each of the first, second and third correlators includes an integrate and dump stage.

8. (Previously Presented) A Rake receiver as claimed in claim 4, characterised in that each of the first and second correlators includes an integrate and dump stage.

9. (Previously Presented) A Rake receiver as claimed in claim 1, characterised by filtering means in the signal path from the combining means.

Please add the following claims:

10. (NEW) A rake receiver comprising:

a radio signal receiving stage;

an analogue-to-digital converter (ADC) coupled to the receiving stage;

the ADC output being coupled to an input of each of a plurality of parallel signal paths each of the parallel signal paths including signal processing means, combining means for combining outputs from the signal paths and means for recovering symbols from the combined outputs;

the receiver further comprising code generation means for generating a filtered pilot code that provides a multibit interpolation of a generated pilot code prior to the parallel signal paths, wherein the code generation means comprises early, on-time and late outputs of the filtered pilot code; and

the signal processing means in each of the parallel signal paths comprising a variable delay means for delaying a signal in that path by a desired amount and a means for correlating the delayed signal with the filtered pilot code, wherein the signal processing means includes signal deriving means coupled to an output of the code generation means and to the variable delay means for deriving an early-late timing error signal for the signal path, wherein the timing error signal is supplied to means for both adjusting the variable time delay of the variable delay means and for deriving an amplitude and phase of the received signal in the respective signal path, and the timing error signal is further supplied to means for multiplying the delayed signal from the variable delay means by the complex conjugate of the amplitude and phase of the received signal and applying the result to the combining means, further wherein the signal deriving means comprises differencing means having inputs connected

respectively to the early and late outputs of the code generation means, first and second correlators, each of the first and second correlators having first and second inputs, the first inputs being coupled to the output of the variable delay means and the second inputs being connected respectively to the on-time output of the code generation means and to an output of the differencing means, the first correlator having an output for the amplitude and phase of the received signal in the signal path and the second correlator having an output for the early-late timing error signal.

11. (NEW) A Rake receiver comprising:

a radio signal receiving stage;

an analogue-to-digital converter (ADC) coupled to the receiving stage;

the ADC output being coupled to an input of each of a plurality of parallel signal paths each of the parallel signal paths including signal processing means, combining means for combining outputs from the signal paths and means for recovering symbols from the combined outputs;

the receiver further comprising code generation means for generating a filtered pilot code that provides a multibit interpolation of a generated pilot code prior to the parallel signal paths, and the signal processing means in each of the parallel signal paths comprising a variable delay means for delaying a signal in that path by a desired amount and a means for correlating the delayed signal with the filtered pilot code, further wherein the signal processing means includes signal deriving means coupled to an output of the

code generation means and to the variable delay means for deriving an early-late timing error signal for the signal path, further wherein the signal processing means includes signal deriving means coupled to an output of the code generation means and to the variable delay means for deriving an early-late timing error signal for the signal path, wherein the timing error signal is supplied to means for both adjusting the variable time delay of the variable delay means and for deriving an amplitude and phase of the received signal in the respective signal path, and the timing error signal is further supplied to means for multiplying the delayed signal from the variable delay means by the complex conjugate of the amplitude and phase of the received signal and applying the result to the combining means, wherein the code generation means comprises early and late outputs of the filtered pilot code, wherein the signal deriving means comprises first and second correlators, each of the first and second correlators having first and second inputs, the first inputs being coupled to the output of the variable delay means and the second inputs being connected respectively to the early and late outputs of the code generation means, differencing means having inputs coupled respectively to outputs of the first and second correlators and an output for the early-late timing error signal and combining means having inputs coupled respectively to outputs of the first and second correlators and an output for the amplitude and phase of the received signal in the signal path.

12. (NEW) The rake receiver as claimed in claim 10, wherein each of the first and second correlators includes an integrate and dump stage.